Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). A method for storing data within a non-volatile memory of a memory system, the method comprising:

identifying a first block into which the data is to be stored;

obtaining an indicator associated with the first block, the indicator having a value indicative of reliability of the first block;

~~determining when~~ responsive to the indicator associated with the first block meeting a criterion, encoding ~~indicates that~~ the data ~~is to be encoded~~ using a first error detection algorithm;

responsive to the indicator associated with the first block not meeting the criterion, encoding the data using ~~the first~~ a second error detection algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm ~~when it is determined that the data is to be encoded using the first algorithm~~; and

then writing the encoded data ~~encoded using the first algorithm~~ into the first block.

2 (canceled).

3 (currently amended). The method of claim ~~2~~ 1 wherein the first error detection algorithm is a 1-bit error correction code (ECC) algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

4 (currently amended). The method of claim ~~2~~ 1 wherein the indicator ~~is arranged to indicate when~~ has a value indicative of whether the block is a reclaimed block~~, wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data is to be encoded using the second algorithm~~.

5 (currently amended). The method of claim ~~2~~ 1 wherein the indicator ~~is arranged to indicate~~ has a value indicative of a number of times the block has been erased.

6 (currently amended). ~~The~~ A method ~~of claim 5 wherein determining when the indicator indicates that the data is to be encoded using the first algorithm includes~~ for storing data within a non-volatile memory of a memory system, the method comprising:

identifying a first block into which the data is to be stored;

obtaining an indicator associated with the first block, the indicator having a value indicative of a number of times the first block has been erased;

determining ~~when~~ whether the indicator is less than a threshold value,

~~wherein when~~ responsive to the indicator ~~is~~ being less than the threshold value, encoding the data ~~is to be encoded~~ using the first algorithm and then writing the data encoded using the first algorithm into the first block; and

responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using the second algorithm into the first block.

7 (currently amended). The method of claim ~~2~~ 1 wherein the indicator ~~is arranged to indicate~~ has a value indicative of an approximately average number of times blocks within the non-volatile memory have been erased.

8 (currently amended). The method of claim ~~2~~ 1 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block,

and wherein obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

9 (original). The method of claim 1 wherein the non-volatile memory is a flash memory.

10 (original). The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

11 (currently amended). ~~A~~ The method ~~for reading data within a non-volatile memory of a memory system, the method~~ of claim 1, further comprising:

identifying ~~a~~ the first block as a block from which data is to be read;

obtaining ~~an~~ the indicator associated with the first block;

~~determining when~~ responsive to the indicator associated with the first block meeting a criterion, decoding ~~indicates that~~ the data stored in the first block ~~has encoded~~ using ~~a~~ the first error detection algorithm; and

responsive to the indicator associated with the first block not meeting the criterion, decoding the data using the ~~first~~ second error detection algorithm ~~when it is determined that the data has been encoded using the first algorithm~~.

12 (canceled).

13 (currently amended). The method of claim ~~12~~ 11 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

14 (currently amended). The method of claim ~~12~~ 11 wherein the indicator ~~is arranged to indicate when~~ has a value indicative of whether the block is a reclaimed block~~, and wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data has been encoded using the second algorithm~~.

15 (currently amended). The method of claim ~~12~~ 11 wherein the indicator ~~is arranged to indicate~~ has a value indicative of a number of times the block has been erased.

16 (currently amended). ~~The~~ A method ~~of claim 15 wherein determining when the indicator indicates that the data has been encoded using the first algorithm includes~~ for reading date within a non-volatile memory of a memory system, the method comprising:

identifying a first block from which data is to be read;

obtaining an indicator associated with the first block, the indicator having a value indicative of a number of times the first block has been erased;

determining ~~when~~ whether the indicator is less than a threshold value,

responsive to ~~wherein when~~ the indicator ~~is~~ being less than the threshold value, decoding the data ~~has been encoded~~ using the first algorithm; and

responsive to the indicator not being less than the threshold value, decoding the data using a second algorithm.

17 (currently amended). The method of claim ~~12~~ 11 wherein the indicator ~~is arranged to indicate~~ has a value indicative of an approximately average number of times physical blocks of the non-volatile memory have been erased.

18 (currently amended). The method of claim ~~12~~ 11 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block,

and wherein obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

19 (original). The method of claim 11 wherein the non-volatile memory is a flash memory.

20 (original). The method of claim 19 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

21 (currently amended). A memory system comprising:

a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block;

code devices for identifying the first block into which data is to be stored;

code devices for obtaining an indicator associated with the first block, the indicator having a value indicative of reliability of the first block;

~~code devices for determining when the indicator indicates that the data is to be encoded using a first algorithm;~~

code devices for encoding the data using ~~the~~ a first error detection algorithm ~~when it is determined that the data is to be encoded using the first algorithm~~ responsive to the indicator meeting a criterion, and for encoding the data using a second error detection algorithm

responsive to the indicator not meeting the criterion, the second error detection algorithm having a higher error detection capability than the first error detection algorithm;

code devices for writing ~~the~~ encoded data ~~encoded using the first algorithm~~ into the first block; and

a memory area that stores the code devices.

22 (canceled).

23 (currently amended). The memory system of claim ~~22~~ 21 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

24 (currently amended). The memory system of claim ~~22~~ 21 wherein the indicator is arranged to indicate ~~when~~ whether the block is a reclaimed block~~, and wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data is to be encoded using the second algorithm~~.

25 (currently amended). The memory system of claim ~~22~~ 21 wherein the indicator ~~is arranged to indicate~~ has a value indicative of a number of times the block has been erased.

26 (currently amended). ~~The~~ A memory system ~~of claim 25 wherein the code devices for determining when the indicator indicates that the data is to be encoded using the first algorithm include~~ comprising:

a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block;

code devices for identifying the first block into which data is to be stored;

code devices for obtaining an indicator associated with the first block, the indicator having a value indicative of a number of times the first block has been erased;

code devices for determining ~~when~~ whether the indicator is less than a threshold value,

code devices for encoding the data using the first algorithm responsive to ~~wherein when~~ the indicator ~~is~~ being less than the threshold value;~~, the data is to be encoded using the first algorithm~~

code devices for writing the data encoded using the first algorithm into the first block;

code devices for encoding the data using a second algorithm responsive to determining that the data is not to be encoded using the first algorithm;

code devices for writing the data encoded using the second algorithm into the first block; and

a memory area that stores the code devices.

27 (original). The memory system of claim 21 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

28 (currently amended). ~~A~~ The memory system of claim 21, further comprising:

~~a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block, the first block including data;~~

~~code devices for identifying the first block;~~

~~code devices for obtaining an indicator associated with the first block;~~

code devices for determining ~~when~~ whether the indicator ~~indicates that the data has been encoded using a first algorithm~~ meets the criterion;

code devices for decoding the data using the first error detection algorithm responsive to the indicator meeting the criterion, and for decoding the data using the second error detection algorithm responsive to the indicator not meeting the criterion ~~when it is determined that the data has been encoded using the first algorithm; and a memory area that stores the code devices~~.

29 (canceled).

30 (currently amended). The memory system of claim ~~30~~ 28 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

31 (currently amended). The memory system of claim ~~30~~ 28 wherein the indicator is arranged to indicate ~~when~~ whether the block is a reclaimed block~~, and wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data has been encoded using the second algorithm~~.

32 (currently amended). The memory system of claim ~~30~~ 28 wherein the indicator ~~is arranged to indicate~~ has a value indicative of a number of times the block has been erased.

33 (currently amended). ~~The~~ A memory system ~~of claim 33 wherein the code devices for determining when the indicator indicates that the data has been encoded using the first algorithm include~~ comprising:

a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block, the first block including data;

code devices for identifying the first block;

code devices for obtaining an indicator associated with the first block, the indicator having a value indicative of a number of times the block has been erased;

code devices for determining ~~when~~ whether the indicator is less than a threshold value,

~~wherein when~~ code devices for decoding the data using a first algorithm responsive to the indicator ~~is~~ being less than the threshold value~~, the data has been encoded using the first algorithm~~.

code devices for decoding the data using a second algorithm responsive to the indicator not being less than the threshold value; and

a memory area that stores the code devices.

34 (currently amended). The memory system of claim ~~29~~ 28 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

Claims 35 through 37 are canceled.

38 (currently amended). A memory system comprising:

a non-volatile memory that includes a first block into which data is to be stored;

~~means that identify the first block;~~

means that obtain an indicator associated with the first block, the indicator having a value indicative of reliability of the first block; ~~means that determine when the indicator indicates that the data is to be encoded using a first algorithm;~~ and

means that encode the data using ~~the~~ a first error detection algorithm ~~when it is determined that the data is to be encoded using the first algorithm~~ responsive to the indicator meeting a criterion, and that encode the data using a second error detection algorithm responsive to the indicator not meeting the criterion, the second error detection algorithm having a higher error detection capability than the first error detection algorithm.

39 (canceled).

40 (currently amended). The memory system of claim ~~40~~ 38 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

41 (currently amended). The memory system of claim ~~39~~ 38 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

42 (currently amended). ~~A~~ The memory system of claim 38, further comprising:

~~a non-volatile memory that includes a first block from which data is to be read;~~

~~means that identify the first block;~~

~~means that obtain an indicator associated with the first block;~~

~~means that determine when the indicator indicates that the data stored in the first block has encoded using a first algorithm; and~~

means that decode the data using the first error detection algorithm ~~when it is determined that the data has been encoded using the first algorithm~~ responsive to the indicator

meeting the criterion, and that decode the data using the second error detection algorithm responsive to the indicator not meeting the criterion.

43 (canceled).

44 (currently amended). The memory system of claim ~~44~~ 42 wherein the first error detection algorithm is a 1-bit ECC algorithm and the second error detection algorithm is a 2-bit ECC algorithm.

45 (currently amended). The memory system of claim ~~43~~ 42 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.